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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Brian J. Buckmeier

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10/24/2007

WOLF BLOCK SCHORR AND SOLIS-COHEN LLP
250 PARK AVENUE
NEW YORK, NY 10177

EXAMINER

THOMAS, LUCY M

ART UNIT

PAPER NUMBER

2836

MAIL DATE

DELIVERY MODE

10/24/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/799,377	Applicant(s) BUCKMEIER ET AL.	
	Examiner Lucy Thomas	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-44 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-11, 17-31, 37-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Acknowledged Prior Art (AAPA) in view of Takazawa et al. (Japanese Patent Application Laid Open No. 2001 060838). Regarding Claim 1, AAPA discloses a connector (see Figures 3-4) comprising at least one pair of contacts J1-J8; at least one pair of terminals P1-P8 electrically coupled to the contacts by at least one pair of conductors; and a transient voltage suppression component electrically coupled to the contacts and said terminals, including a transient voltage suppression device (TVS) 310 having a capacitance. AAPA does not disclose a frequency compensation device, wherein the frequency compensation device is effective to neutralize the capacitance of the transient voltage suppression device.

Takazawa et al. discloses a transient voltage suppression component (see Figures 1, 4) comprising a transient voltage suppression device (see varistor 2) and a frequency compensation device (see inductor 4), and the inductor would perform the frequency compensation to neutralize the capacitance of the transient voltage suppressor (impedance of inductance and capacitance varies with frequency, ω as, $Z_L = j \omega L$ and $Z_C = i/j \omega c$ and the in the total impedance of the system, frequency

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components of inductive and capacitive elements compensate each other). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the connector of AAPA and to provide a frequency compensation device as taught by Takazawa, to alleviate the effects of the capacitance of the TVS device and/or parasitic capacitance, and to have transient voltage (static charge/electricity) suppression with a little distortion in the waveform of a high frequency signal (see Takazawa, Abstract).

Regarding Claim 2, Takazawa discloses that the frequency compensator device is coupled in series with the transient voltage suppression device.

Regarding Claim 3, AAPA discloses the transient voltage suppression component is coupling the pair of conductors.

Regarding Claim 4, Takazawa discloses that the frequency compensation device is an inductor (see inductor 4 in Figure 1).

Regarding Claim 5, AAPA discloses that the transient voltage suppression components are used for each pair of conductors (see 310 connected to conductors from P3, P6 and P7, P8).

Claim 6 recites the connector, wherein two of said transient voltage suppression devices and two of said frequency compensation devices are used for each pair of conductors. It would be obvious to one of ordinary skill in art to use summation of circuit elements to satisfy the power rating requirements of the system. Claim 7 only recites basically Claim 2 and Claim 6 combined, and does not add any further limitation, as Claim 2 has already limited the elements to be in series. Claim 8 basically recites Claim

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6, except that it additionally recites that said frequency compensation devices are coupled to ground, which is a common practice in the art to provide a safety path to the undesired signals to ground. The first part of Claim 9 basically recites Claim 6, except using a broader limit of a set of elements, instead of 2 elements. The second part of Claim 9, and Claim 10 basically adds plurality of set of elements. It would be obvious to those skilled in art to use summation of circuit elements to satisfy the power rating requirements of the system. The additional recitation of how the set of elements are coupled does not add any limitation as the Claim 2, already limits the elements to be in series connection.

Regarding Claim 11, AAPA discloses a filter component 254 electrically coupled to the pair of conductors.

Regarding Claim 17, transient voltage suppression device 310 of AAPA and varistor 2 of Takazawa protect against electrostatic discharge.

Regarding Claim 18, AAPA discloses the connector, wherein said transient voltage suppression device protects against differential voltage surges (see Figure 4, Specification, Page 6, lines 10-12). Regarding Claim 19, the transient voltage suppression devices of both AAPA and Takazawa, protect against voltage surges above a certain threshold. Claim 20 only recites the function of an inductor as an energy storage device, which is inherently performed by the inductor.

Claims 21-25 basically recite the elements of Claims 1-5, except that a transient voltage suppression component is claimed for use in a connector. The rejection of Claims 1-5 would apply as the above mentioned connector provides a transient voltage

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suppression component. Claim 31 recites the elements of Claim 11, Claims 26-30 recite the elements of Claim 6-10, and Claims 37-40 recite the elements of Claims 17-20 for the transient voltage suppression component used in the connector. Claim 41 recites a circuit with the recited elements of Claim 1. Regarding Claim 42, Takazawa discloses that the transient voltage suppression component is inductively coupled to conductors connected to 10 and 11. Regarding method Claims 43-44, the recited steps would necessarily be performed when using the connector as recited in Claims 1-2, and therefore may be rejected on the same basis as Claims 1-2.

3. Claims 12-16 and 32-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Acknowledged Prior Art (AAPA) in view of Takazawa et al. (Japanese Patent Application Laid Open No. 2001 060838) and Hershfield (US 4,677,518). Regarding Claims 12-15, neither AAPA or Takazawa disclose a voltage suppression device which includes a varistor as recited in Claim 12, or a Zener as recited in Claim 13, or a diode as recited in Claim 14, or a current limiting device as recited in Claim 15. Hershfield discloses a voltage suppression device, which includes a varistor (see 14 in Figure 1, 44,50,58 in Figure 4, 110, 112 in Figure 6, Column 1, lines 6-15), a Zener diode (see 34 in Figure 3, Column 3, lines 67-69), a diode (see 128 in Figure 6), and current limiting device (see 36 in Figure 3). It would be obvious to one of ordinary skill in the art to include the above-recited elements in a voltage suppression device as taught by Hershfield, as these elements are known to protect electrical systems from transient voltages. Zener diode and varistor limit the amplitude of voltage transients applied to the electrical equipment being protected, a current limiting element

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protects other components of a protection circuit from damage by excessive current, and using varistor as a current limiting element has the added advantage that the voltage across the combination of elements at high currents. Claim 16 only adds functional limitation of a Zener diode or diode recited in Claim 13-14. Claims 32-36 recite the elements of Claims 12-16 for the transient voltage suppression component for use in the connector.

Response to Arguments

4. Applicant's arguments filed on 7/18/2007 have been fully considered.

Regarding Applicant arguments toward Takazawa reference: Takazawa discloses a transient voltage suppression device (see varistor 2) and a frequency compensation device (see inductor 4), and the inductor would perform the frequency compensation to neutralize the capacitance of the transient voltage suppressor. Impedance of inductive and capacitive elements varies with frequency, ω as, $Z_L = j \omega L$ and $Z_C = i/j \omega c$ and thus the in the total impedance, frequency components of inductor and capacitance compensate each other. Waveform or signal amplitude of a system depends on the impedance of the system, and distortion or unwanted voltage variation can occur if the (parasitic/unwanted) capacitance are uncompensated, and the inductor of Takazawa compensate the parasitic capacitance or capacitance of the surge suppressor.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucy Thomas whose telephone number is 571-272-6002. The examiner can normally be reached on Monday - Friday 8:00 AM - 4:30 PM EST.

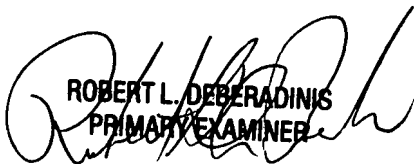
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LT

October 18, 2007


ROBERT L. DEBERADINIS
PRIMARY EXAMINER